

# NTSC/PAL Encoder

## SILICON INTELLECTUAL PROPERTY SOLUTION

### OVERVIEW

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The NTSC/PAL Encoder Core is capable of producing video signals to drive NTSC or PAL compatible video monitors. The input is either 8-bit or 16-bit luma and chroma pixel data. The encoder performs the necessary filtering, synchronization generation, and interpolation of the data. The outputs can be interfaced directly to D/A converters for generation of analog video signals. The encoder also supports Macrovision™ Copy Protection Revisions 7.1.L1 and 1.2, encoding of closed captioning data, wide screen signaling, and copy generation management.

### FEATURES

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- Composite, S-Video, and Component video outputs
- Programmable Component matrix
- Supports NTSC, NTSC-Japan, PAL (M, N, B, G, H, I, D) and PAL-60 standards
- Compatible with 8-bit/16-bit parallel CCIR-601/CCIR656 input formats
- Selectable master or slave synchronization mode
- Built-in video color bar test generator
- Line 21 Closed Caption encoding
- Macrovision™ Revision 7.1.L1 support
- Support for Copy Generation Management and Wide Screen Signaling
- 27 MHz interpolated outputs

### STANDARDS COMPLIANCE

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- ITU-R B.601 “Studio Encoding Parameters of Digital Television For Standard 4:3 and Wide-Screen 16:9 Aspect Ratios”
- ITU-R B.656 “Interfaces for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601 (Part A)”
- EIA/CEA 608-B Line 21 Data Services
- EIA/IS-702 Copy Generation Management System (Analog)
- EN 300 294 “Television Systems: 625-Line Television Wide Screen Signaling (WSS)”
- SMPTE 125M-1995 “Television – Component Video Signal 4:2:2 – Bit-Parallel Digital Interface”
- IEC 61880-2 Video Systems (525/60) – Video and Accompanied Data Using the Vertical Blanking Interval – Analogue Interface Part 2: 525 Progressive Scan System

## APPLICATIONS

- Digital cameras and camcorders
- Digital cable set top boxes

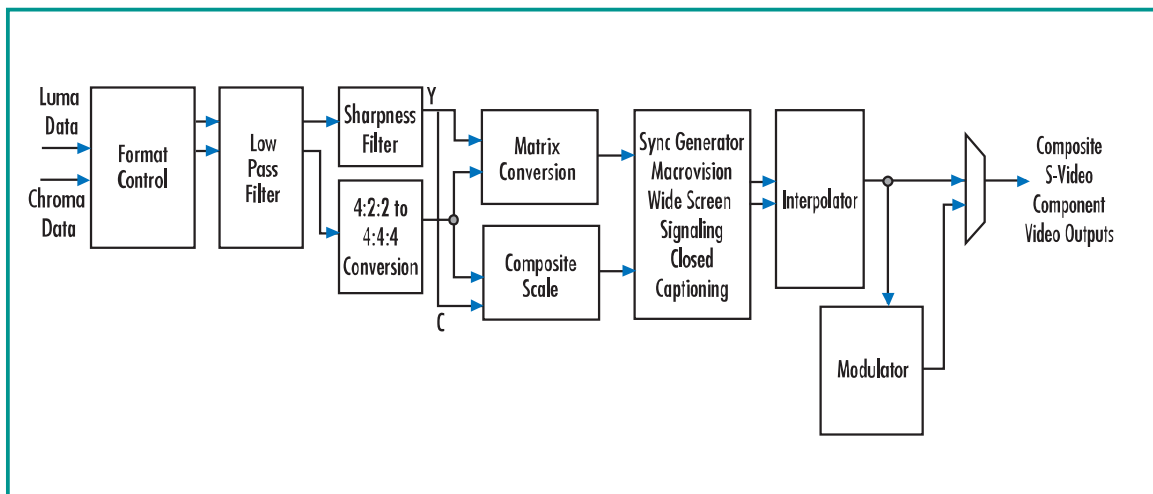
## DESIGN PACKAGE

- Verilog® Source Code
- Verilog® Test Bench
- Microarchitecture Specifications
- Engineering support for technology transfer

## OPTIONAL FEATURES

- Progressive Component Output (NTSC only)
- Macrovision™ Revision 1.2 (525p only)
- 54 MHz interpolated outputs
- 10-bit D/A converter for interlaced or progressive outputs
- Altera FPGA net list

## BLOCK DIAGRAM



Verilog is a registered trademark of Cadence Design Systems, San Jose, CA.

### For more information, contact:

Sarnoff Corporation  
201 Washington Road  
PO Box 5300, Princeton, NJ 08543  
Phone: (609) 734-2553, Fax: (609) 734-2040  
www.sarnoff.com  
e-mail: bd@sarnoff.com

